

中原大學 97 學年度碩士班入學考試

4 月 13 日 14:00~15:30 電子工程學系
數位與類比系統組(乙組)

誠實是我們珍視的美德，
我們喜愛「拒絕作弊，堅守正直」的你！

科目：數位電路

(共 1 頁第 1 頁)

可使用計算機，惟僅限不具可程式及多重記憶者 不可使用計算機

- [15%] Do the followings:
 - Use Karnaugh Map to find a **minimum sum-of-products** expression for the function $F(A,B,C,D,E) = \sum m(0,1,6,10,12,14,16,17,26,30)$, which is in minterm expansion.
 - Plot** the circuit using only **NAND** gates.
- [10%] Use an **8-to-1 multiplexer** and some **inverters** to implement the function $F(A,B,C,D) = \Pi M(0,2,5,7,8,10,13,15) \cdot \Pi D(2,3)$, which is in maxterm expansion.
- [15%] Assume you have inverters, AND and OR gates, multiplexers, and 1-bit full adders. **Plot** a **2's complement 4-bit adder/subtractor with an overflow output** using only these parts. The overflow output should be "0" if no overflow occurred and be "1" if an overflow occurred. The inputs of the adder/subtractor are signed numbers $(A_3, A_2, A_1, A_0, B_3, B_2, B_1, B_0)$ and Add_Sub. The outputs are $(\text{Overflow}, S_4, S_3, S_2, S_1, S_0)$.
- [20%] For edge-triggered flip-flops,
 - Plot the **truth tables** of **S-R**, **D**, **T**, and **J-K** flip-flops.
 - How to add some suitable gates externally to convert a **J-K** flip-flop to a **T** flip-flop?
 - How to add some suitable gates externally to convert a **T** flip-flop to a **J-K** flip-flop?
- [15%] Use **J-K** flip-flops and **logic gates** to implement a **4-bit synchronous counter**, counting from 0000 to 1111 and returning to 0000 after 1111.
- [25%] For the following state diagram,
 - Minimize it to a **minimum state transition table**, i.e. with the fewest states.
 - Write a **Verilog** or **VHDL** file to describe this circuit.

