

中原大學 96 學年度碩士班入學考試

96/03/25 16:00~17:30 資訊工程學系

誠實是我們珍視的美德，
我們喜愛「拒絕作弊，堅守正直」的你！

科目：計算機系統(含作業系統與計算機組織)

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不可使用計算機

1. Explain the following Terminologies. (15%)
 - 1) Virtual Machine
 - 2) Pipe
 - 3) Gantt Chart

2. The program to solve the critical section problem is shown in the following, and the swap() instruction is implemented by the hardware. (20%)

```
key = true;
repeat
    swap(lock,key);
until key = false;
```

CRITICAL SECTION

```
lock = false;
```

- 1) What is the meaning of the swap() instruction is implemented by the hardware?
 - 2) Prove the program that satisfies mutual exclusion.
 - 3) Do you agree that the program satisfies progress and bounded waiting? Why?
 - 4) Please give a program to solve the critical section problem, and satisfies mutual exclusion, progress and bounded waiting.

3. Please answer the following file system problems. (15%)
 - 1) Explain the purpose of the open file and close file operations.
 - 2) Some systems automatically open a file when it is referenced for the first time, and close the file when the job terminates. Discuss the advantages and disadvantages of this scheme as compared to the more traditional one, where the user has to open and close the file explicitly.
 - 3) Please draw a diagram to show the file allocation scheme and free space management for File Allocation Table (FAT).

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4. Please define the following term: (15%)
 - 1) Pipeline Hazards
 - 2) Branch Prediction
 - 3) Superscalar
 - 4) Simultaneous Multithreading
 - 5) Chip Multiprocessor

5. Please design and implement “Multi-Cycle MIPS-Lite Processor” with eight instructions: “add”, “sub”, “and”, “or”, “lw”, “sw”, “beq”, “j”, according to the following questions: (35%)
 - 1) Please draw the complete datapath for the processor. (5 %)
 - 2) Please implement the datapath by using Verilog HDL. (10 %)
 - 3) Please use Finite State Machine (FSM) to design the corresponding control unit according to your datapath, and then draw the state diagram. (5 %)
 - 4) Please implement the FSM by using Verilog HDL. (10 %)
 - 5) Please integrate the Verilog codes of datapath and FSM to a whole MIPS-Lite CPU, and then provide a testbench to verify its correctness. (5 %)