

中原大學 94 學年度碩士班入學考試

3 月 20 日 16:00~17:30 資訊工程系

誠實是我們珍視的美德，
我們喜愛「拒絕作弊，堅守正直」的你！

科目：計算機系統

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可使用計算機，惟僅限不具可程式及多重記憶者

不可使用計算機

1. Explain the following Terminologies. (15%)
 - 1) File Attributes
 - 2) Deadlock
 - 3) Multilevel Feedback Queue
 - 4) Trap
 - 5) Context Switch

2. Please answer the following paging scheme and virtual memory problems. (16%)
 - 1) Draw a diagram then explain how to map logical address to physical address. (6%)
 - 2) The size of one page is 4KB, and one logical address 7315F46 is mapped to physical address 315F46, please calculate page number and frame number. (4%)
 - 3) On the average, how many pages of internal fragmentation for each process will be wasted? (3%)
 - 4) Which schemes may have internal fragmentation? (3%)
 - a. Variable Partition
 - b. Relocatable Fixed Partition
 - c. Segmentation
 - d. Segmentation with Paging

3. Please answer the following semaphore problems. (19%)
 - 1) A semaphore S is an integer variable that can be operated upon only by the atomic operations: wait and signal. Explain what is meant of the term atomic operation. (3%)
 - 2) Define wait and signal by using block and wakeup functions. (6%)
 - 3) Binary semaphore S can be used to control the access to shared data, give an example to show this synchronization problem, and explain possible values of S in your example. (5%)
 - 4) Prove your example satisfies mutual exclusion, progress, and bounded waiting requirements. (5%)

4. (5%) Design a combinational circuit which takes a 4-bit unsigned number as input and gives its modulo 3 residue as output. (For example, the circuit outputs 10_2 when the input is 1000_2)
 - a. Construct the truth table for the circuit.
 - b. Find the minimized Boolean expression for each output bit.

5. (15%) Design a digital circuit that reads in as many numbers as possible until the sum of the even number inputs is bigger than that of the odd number inputs, then outputs the number of the numbers that has been read.
- Develop an algorithm for the processing procedure.
 - Design a simple datapath with control signals identified.
 - Define the controller with a state machine and give an implementation of the controller
6. (15%)
- Briefly explain what TLB is and what function it provides.
 - Suppose a system with a 256-byte page size and a 64-entry direct-mapped cache with a 1-word block size. There are three entries in its TLB. Draw a diagram to show an implementation of the memory subsystem containing the TLB and the cache with all connecting signal lines marked with its width.
 - After it is up and running for sometime, now its TLB contains the following tag and physical page number pair: (8, 3), (9, 11), (10, 4). All valid bits and dirty bits of the TLB are set (i.e. all entries are valid and the corresponding page is dirty). Here is a series of address references in word addresses : 2049, 2305, 2561. If the first reference is a hit, can you determine whether the 2nd is a hit or a miss? Why? How about the 3rd reference?
7. (15%) Consider a load-store machine with a 6-stage pipeline:

IF	Instruction fetch
ID	Instruction decode
RF	Register files accessed, branch detection completed
EX	ALU operation performed, data address calculated
M	Data access completed
W	Write result back to register file

Suppose all possible data forwarding circuits are present. Given the following code fragment, illustrate, using timing diagram, how each instruction progress through the pipeline during the last two cycles of the loop until the execution leaves the loop. Identify all the hazards and indicate how they are resolved in your answer.

```

Loop:  sub   $2, $2, $1    /* $2=$2-$1
        lw    $5, 0($2)   /* $5=Mem[$2+0]
        lw    $6, 1000($2) /* $6=Mem[$2+1000]
        add   $7, $5, $6  /* $7=$5+$6
        bne   $2, $3, Loop /* if $2 <> $3 go to Loop
        sw    $7, 2000($2) /* Mem[$2+2000] = $7
        add   $7, $8, $7  /* $7 = $8+$7
        sub   $4, $8, $6  /*$4 = $8-$6
    
```